CBCS SCHEME

USN | | | | | | | | | |

BEC654A

Sixth Semester B.E./B.Tech. Degree Examination, June/July 2025
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain typical design flow for designing VLSI IC circuits with a neat diagram.	10	L2	CO1
	b.	Explain the popularity of verilog HDL.	5	L1	CO1
	c.	Explain the different levels of abstraction used in verilog modeling.	5	L1	CO1
		OR			
Q.2	a.	Explain design hierarchy of 4 bit Ripple carry counter and also list the design methodology.	10	L2	CO1
	b.	Explain components of simulation with proper diagram.	6	L1	CO1
	c.	List the trends in HDL.	4	L1	CO1
		Module – 2			
Q.3	a.	List all data types and explain Vectors, Arrays, Memories and Parameters with example.	10	L1	CO2
	b.	Briefly explain \$monitor, \$display with one example and also list string format specifications.	10	L1	CO2
		OR			
Q.4	a.	Discuss components of the verilog module with a neat diagram.	8	L1	CO2
	b.	Mention types of connecting ports and explain each with example.	6	L1	CO2
	c.	Explain compiler directives.	6	L1	CO2
		Module – 3			
Q.5	a.	Write block diagram and truth table of Bufif and Notif logic gates.	6	L1	CO3
	b.	Write a verilog program for 4:1 multiplexor using gate level modeling. Also write truth table and circuit diagram.	8	L2	CO3
	c.	Evaluate the following if A = 1′b1 ; B = 2′b00 ; C = 2′b10 ; D = 5; E = 3; F = 4′b0000 ; G = 4′b1111; i) Y = {4{A}, 2{B}, C} ii) D/E iii) D %E iv) F ~ ∧ G v) B = = C vi) \$F	6	L2	CO3

		OR			
Q.6	**a.**	List all operator types and symbols with neat table.	**8**	**L1**	**CO3**
	b.	Explain conditional operator with suitable example.	**4**	**L2**	**CO3**
	c.	Write 4 bit full adder with carry look ahead program.	**8**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Explain blocking and non-blocking statements with examples.	**8**	**L2**	**CO3**
	b.	Write the syntax of CASE statements. Also list the types of CASE statements implement 4:1 multiplexor using case statement.	**4**	**L2**	**CO3**
	c.	List all the loop statements. Explain any two loop statements with example.	**8**	**L2**	**CO3**
		OR			
Q.8	**a.**	Write behavioral program for 4-bit counter.	**4**	**L1**	**CO3**
	b.	Explain about structured procedures.	**8**	**L2**	**CO3**
	c.	Explain the block types with example.	**8**	**L2**	**CO3**
		Module – 5			
Q.9	**a.**	Write a verilog program of full adder using two half adder. Use structural modeling.	**4**	**L2**	**CO4**
	b.	Explain binding between two modulus.	**8**	**L2**	**CO4**
	c.	Explain 2:1 multiplexor logic diagram truth table and also write verilog program.	**8**	**L2**	**CO4**
		OR			
Q.10	**a.**	List the difference between tasks and functions.	**4**	**L1**	**CO4**
	b.	Explain the syntax of task declaration and invocation.	**8**	**L2**	**CO4**
	c.	Write a verilog program that calculates the parity of a 32 bit address. Use function.	**8**	**L2**	**CO4**

* * * * *